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SIMULATION AND COMPARISON OF NEWLY DESIGNED MUTISTRING MULTILEVEL INVERTER WITH HIGH LEVEL INVERTER

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ABSTRACT

This paper presents a single-phase multi-string multilevel inverter for micro grid applications. The multilevel topology consists of few H-bridges connected in series, each one connected to a string. The proposed multistring multilevel inverter needs only six switches whereas conventional cascaded H-bridge multilevel inverter need eight switches. The multi-string inverter topology offers advantages like quality output waveform, small LC filter size, lower total harmonics distortion (THD) and less electromagnetic interference (EMI). The multilevel converters achieve high-voltage switching by means of a series of voltage steps, each of which lies within the ratings of the individual power devices. This paper presents comparison of single-phase Multistring multilevel inverter with single phase high level inverters.

A micro grid has larger power capacity and is able to provide a coordinated integration of the increasing share of distributed generation units in the network. The unique feature of the multilevel inverters is to provide high switching frequencies with low switching losses.

The studied multistring inverter topology offers strong advantages such as improved output waveforms, smaller filter size, and lower electromagnetic interference and total harmonics distortion. The simulation results are verified by Matlab/Simulink software.

KEYWORDS: Multistring Multilevel Inverter, Micro Grid, H-Bridges, Total Harmonics Distortion (THD)

INTRODUCTION

Micro grid is a small scale power supply network that is designed to provide power for a small community. Both renewable and non renewable energy sources can be used in micro grid. Multistring multilevel inverters are used to obtain the sinusoidal output voltage and to reduce the total harmonic distortion by employing less number of switches. In the present scenario the distributed energy resource (DER) based single-phase inverter is usually adopted in the micro grid systems. In order to reduce conversion losses, the key is to save costs and size by removing any kind of transformer as well as reducing the power devices.

A single-phase multistring five-level, seven, nine and eleven level inverter integrated with an auxiliary circuit was recently proposed for DC/AC power conversion. This report presents comparison of newly designed multistring multilevel inverter topology with high level inverters. The new topology produces a significant reduction in the number of power devices and capacitors required to implement a multilevel output.

The new topology achieves a 37.5% reduction in the number of main power switches. Multilevel converters were used only in some high power applications such as high power motor drivers in marine, mining, or chemical industries applications, high power transmission, power line conditioners. Multilevel converters offer high power capability,

associated with lower output harmonics and lower commutation losses.

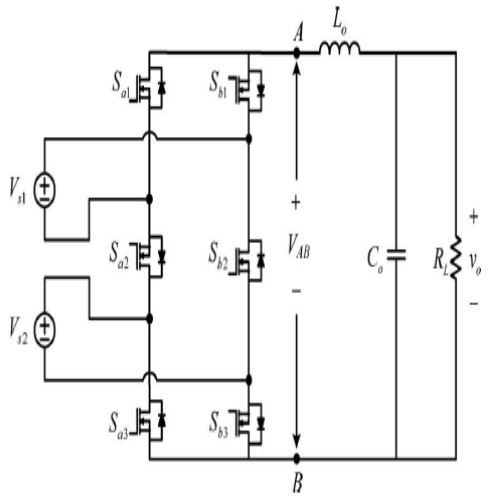

Figure 1: Basic Structure of Multistring Multilevel Inverter

Various topologies for multilevel inverters have been proposed in the literature. Common ones are diode-clamped, flying capacitor or multi-cell, cascaded H-bridge, and modified H-bridge multilevel. Cascaded multilevel inverters synthesize a medium-voltage output by a series connection of power cells which use standard low-voltage component configurations. This feature gives benefit of high-quality output voltages and input currents and also outstanding availability due to their intrinsic component redundancy.

SYSTEM CONFIGURATION OF OPERATION PRINCIPLES

A Full H-Bridge

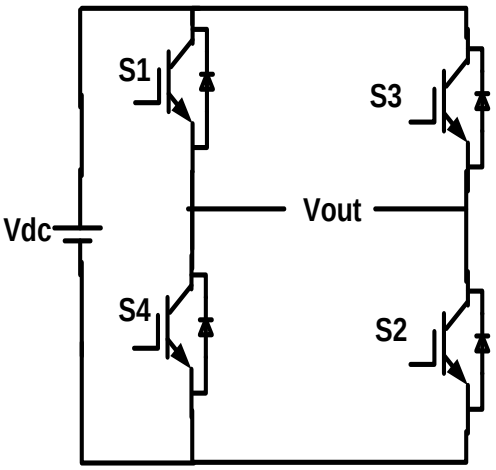

Figure 2: Full H-Bridge

Figure 2 shows the Full H-Bridge Configuration. By using single H-Bridge we can get 3 voltage levels. The number output voltage levels of cascaded Full H-Bridge are given by 2n+1 and voltage step of each level is given by Vdc/n. Where n is number of H-bridges connected in cascaded. The switching table is given in Table 1.

Table 1: Switching Table for Full H-Bridge

Switches Turn ON	Voltage Level
S1,S2	Vdc
S3,S4	-Vdc
S4,D2	0

Simplified Multilevel Inverter Stage

A new single-phase multi string topology, presented as a new basic circuitry in Figure 3. Referring to Figure 2, it should be assumed that, in this configuration, the two capacitors in the capacitive voltage divider are connected directly across the dc bus, and all switching combinations are activated in an output cycle. The dynamic voltage balance between the two capacitors is automatically controlled by the preceding high step-up converter stage. Then, we can

Assume $Vs1 = Vs2 = Vs$

This topology includes six power switches—two fewer than the CCHB inverter with eight power switches—which drastically reduces the power circuit complexity and simplifies modulator circuit design and implementation. . The phase disposition (PD) PWM control scheme is introduced to generate switching signals and to produce five output-voltage levels: 0, VS, $2VS$, $-VS$, and $-2VS$.

This inverter topology uses two carrier signals and one reference to generate PWM signals for the switches. The modulation strategy and its implemented logic scheme is widely used alternative for PD modulation. With the exception of an offset value equivalent to the carrier signal amplitude, two comparators are used in this scheme with identical carrier signals Vtri1 and Vtri2 to provide high-frequency switching signals for switches $Sa1$, $Sb1$, $Sa3$, and $Sb3$. Another comparator is used for zero-crossing detection to provide line-frequency switching signals for switches $Sa2$ and $Sb2$.

The required five output levels and the corresponding operation modes of the multi level inverter stage are described clearly as follows.

- Maximum positive output, $2VS$: Active switches Sa 2, Sb 1, and Sb 3 are ON; the voltage applied to the LC output filter is $2VS$.
- Half-level positive output, $+Vs$: This output condition can be induced by two different switching combinations. One switching combination is such that active switches Sa 2, Sb 1, and Sa 3 are ON; the other is such that active switches Sa 2, Sa 1, and Sb 3 are ON. During this operating stage, the voltage applied to the LC output filter is $+Vs$.
- Zero output, 0: This output condition can be formed by either of the two switching structures. Once the left orright switching leg is ON, the load will be short-circuited, and the voltage applied to the load terminals.
- Half-level negative output, $-Vs$: This output condition can be induced by either of the two different switching combinations. One switching combination is such that active switches Sa 1 , Sb 2 , and Sb 3 are ON; the other is such that active switches Sa 3 , Sb 1 , and Sb 2 are ON.
- Maximum negative output, $-2Vs$: During this stage, active switches Sa 1 ,Sa 3 , and Sb 2 are ON, and the voltage applied to the LC output filter is $-2Vs$

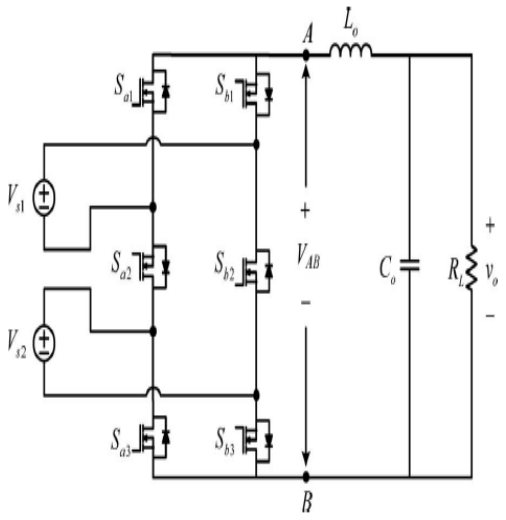

Figure 3: Basic Five-Level Inverter Circuitry

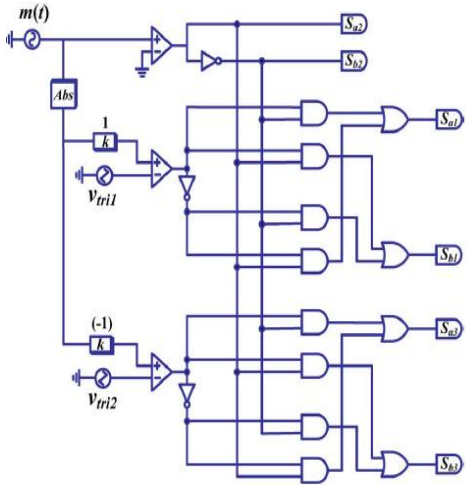

Figure 4: Modulation Logic

MATLAB/SIMULINK MODEL & SIMULATION RESULTS

Diode Clamped Multilevel Inverter

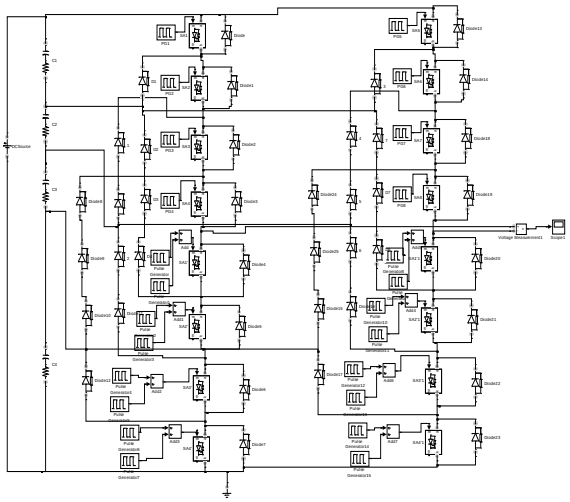

Figure 5: Diode Clamped Multilevel Inverter

The basic simulation circuit shown in Figure 5 is a Eleven level Diode clamped Multilevel inverter with combination of twenty switches in the circuit output voltage are obtained.

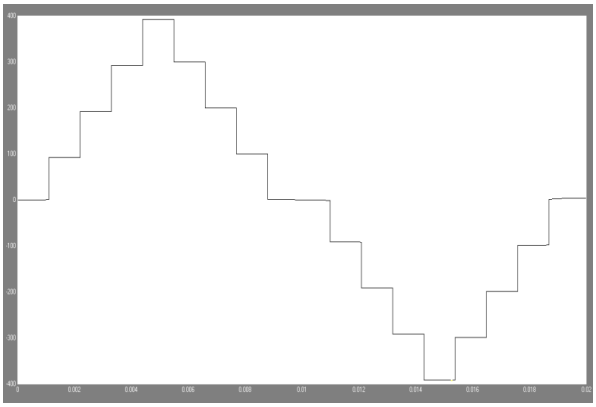

Figure 6: Diode Clamped Multilevel Inverter Output Waveform

Figure 6 shows the output voltage wave form which are obtained by Diode Clamped Multilevel Inverter Output waveform.

Single Phase 11- Level Flying Capacitor Multilevel Inverter

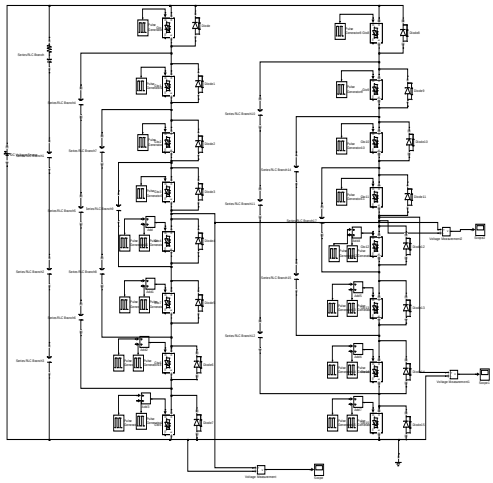

Figure 7: Flying Capacitor Multilevel Inverter

The basic simulation circuit shown in Figure 7 is a Eleven level Flying Capacitor Multilevel inverter with combination of twenty switches in the circuit output voltage are obtained.

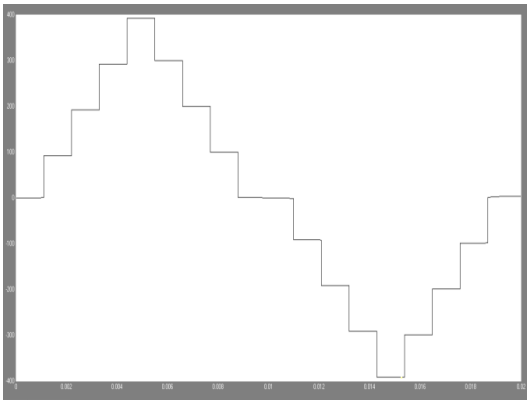

Figure 8: Flying Capacitor Multilevel Inverter Output Waveform

Figure 8 shows the output voltage wave form which are obtained by Flying capacitor Multilevel Inverter Output waveform.

Single Phase 11- Level H-Bridge Inverter

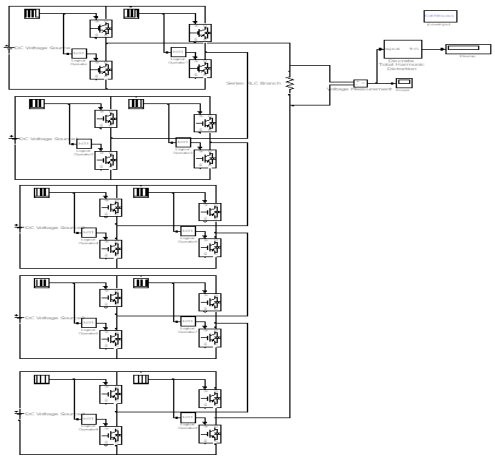

Figure 9: Single Phase Eleven Level H-Bridge Inverter

The basic simulation circuit shown in Figure 9 is a Eleven level Cascaded H-Bridge Multilevel inverter with combination of twenty switches in the circuit output voltage are obtained.

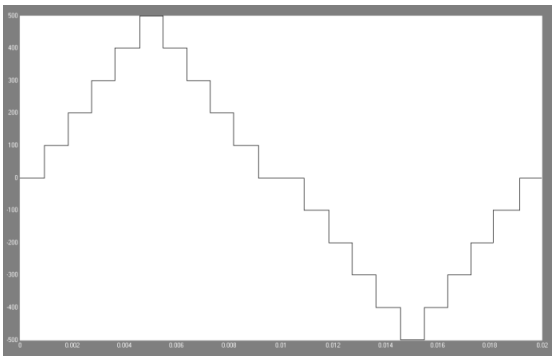

Figure 10: Single Phase Eleven Level H-Bridge Inverter Output Waveform

Figure 10 shows the output voltage wave form which are obtained by Cascaded H-Bridge Multilevel Inverter Output waveform.

Single Phase 11-Level Multistring Multilevel Inverter

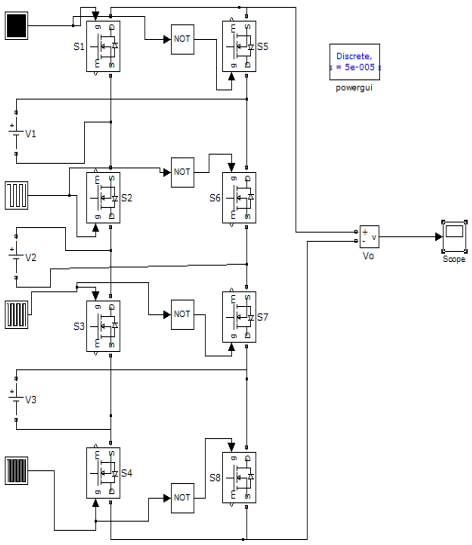

Figure 11: Single Phase 11-Level Multistring Multilevel Inverter

The basic simulation circuit shown in Figure 11 is a Eleven level Newly designed Multi string Multilevel inverter with combination of eight switches in the circuit output voltage are obtained.

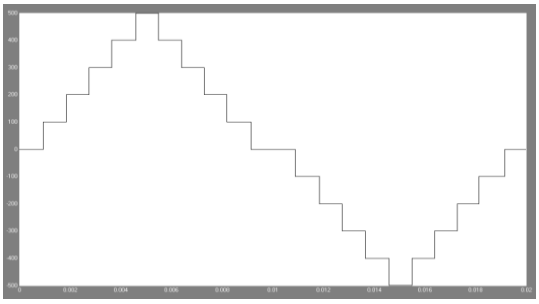

Figure 12: Single Phase Eleven Level Multistring Multilevel Inverter Output Waveform

Figure 12 shows the output voltage wave form which are obtained by Newly designed Multi string Multilevel Inverter Output waveform.

COMPARISON BETWEEN DIFFERENT MULTI LEVEL INVERTER TOPOLOGIES

Comparison between Different Five Level Inverter Topologies

Table 2: Comparison between Different Five Level Inverter Topologies

Multilevel Inverter	Diode Clamped	Flying Capacitor	H-Bribge	Multistring Multilevel
Main controlled switches	8	8	8	6
Auxiliary controlled switches	0	0	0	0
Clamping Diodes	12	0	0	0
Balancing Capacitors	0	10	0	0

Comparison between Different Seven Level Inverter Topologies

Table 3: Comparison between Different Seven Level Inverter Topologies

Multilevel Inverter	Diode Clamped	Flying Capacitor	H-Bribge	Multistring Multilevel
Main controlled switches	12	12	12	6
Auxiliary controlled switches	0	0	0	0
Clamping Diodes	30	0	0	0
Balancing Capacitors	0	15	0	0

Comparison between Different Nine Level Inverter Topologies

Table 4: Comparison between Different Nine Level Inverter Topologies

Multilevel Inverter	Diode Clamped	Flying Capacitor	H-Bribge	Multistring Multilevel
Main controlled switches	16	16	16	8
Auxiliary controlled switches	0	0	0	0
Clamping Diodes	56	0	0	0
Balancing Capacitors	0	28	0	0

Comparison between Different Eleven Level Inverter Topologies

Table 5: Comparison between Different Eleven Level Inverter Topologies

Multilevel Inverter	Diode Clamped	Flying Capacitor	H-Bribge	Multistring Multilevel
Main controlled switches	20	20	20	8
Auxiliary controlled switches	0	0	0	0
Clamping Diodes	90	0	0	0
Balancing Capacitors	0	45	0	0

From the above tables 2,3,4,5 the numbers of switching devices are reduced greater in Multistring Multilevel inverter using auxiliary controlled switch. When the switching devices are reduced the switching losses also reduced then the efficiency of the inverter is improved. In this papet, we proposed model simulated different levels of inverters and compared to other level inverters.

COMPARISON BETWEEN DIFFERENT MULTI LEVEL INVERTER TOPOLOGIES FOR DIFFERENT LOADS

In this project different topologies of multilevel inverters like Diode clamped, flying capacitor and cascaded H-bridge and Multi string Multilevel inverter analysis (for 50HZ) is carried out for various levels along with their corresponding circuit diagrams and waveforms. The total THD of different multi level inverters are tabulated below:

Table 6: Comparison between Different Levels Inverter Topologies for Different Loads

INVERTER	R-Load For 50Hz	RL-Load For 50Hz
1-Ø PWM Inverter	1.478	1.6669
1-Ø Half bridge Inverter	0.4803	0.4817
1-Ø Full Bridge Inverter (3-level)	0.4803	0.4821
1-Ø Diode Clamped Inverter (5-level)	0.2673	--
1-Ø Flying capacitor Inverter (5-level)	0.2637	--
1-Ø H-Bridge Inverter (5-level)	0.5695	0.5721
1-Ø H-Bridge Inverter (7-level)	0.3105	0.3189
1-Ø H-Bridge Inverter (9-level)	0.2576	0.2568
1-Ø H-Bridge Inverter (11-level)	0.2230	0.2223
1-Ø Multistring Multilevel Inverter (5-level)	0.5595	0.5618
1-Ø Multistring Multilevel Inverter (7-level)	0.2439	0.2459
1-Ø Multistring Multilevel Inverter (9-level)	0.1813	0.1832
1-Ø Multistring Multilevel Inverter (11-level)	0.1383	0.1395

From the above results the Total Harmonic Distortion of different multilevel inverters are are compared for different loads. From the above table the total harmonic distortion is reduced, when the level of the inverter is increased.

CONCLUSIONS

In this project the advantages and applications of multilevel inverters are mentioned and a detailed description of different multilevel inverter topologies are presented., and also concluded that controlling of voltage magnitude of inverter by PWM technique is most efficient when compared with other techniques. All these inverter topologies are virtually simulated using MATLAB SIMULINK and the gating signals of different inverter topologies have been analyzed and respective output voltage waveforms are given. From the simulation results, concluded that the non linear loads have reduced total harmonic distortion (THD) in multi level inverters as compared to other conventional inverters. Then the reduced harmonic distortion reduces the switching losses for higher frequency applications. Then the power transfer capability is increased for non linear loads. The conventional inverter eliminates the 3^{rd} harmonic and 5^{th} harmonics in the output voltage.

A brief Comparison of different multilevel inverter topologies are given and we observe that the THD of the output voltage wave is reduced with level improvement of inverter. The Multistring Multilevel inverter gives good performance as compared to other high voltage inverter. We hereby conclude that multilevel inverter is a very promising technology in the power industry.

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